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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,606	12/28/2001	James D. Gallia	TI-32942 (032350.B365)	3751

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EXAMINER	
HU, SHOUXIANG	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,606	GALLIA ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *12-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Claims 12-16 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 3.

Claim Objections

2. Claims 8 and 18 are objected to because of the following informalities and/or defects:

3. In claim 8, the term of "a second one" should read as: --a third one--.

4. In claim 18, the term of "the diode circuit" lacks sufficient antecedent basis in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 4 and 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Staab et al. ("Staab"; US 5,567,968).

Staab discloses a silicon-on-insulator semiconductor device (Figs. 4-9, also see col. 2, line 39, through col. 3, line 40, and col. 6, lines 45-67), comprising: an insulative layer (501, 601, or 801, which is naturally formed overlying a substrate, since it is formed in an SOI structure (see col. 3, lines 25-31, or col. 6, lines 50-52)); an SOI MOSFET (either the P-channel MOSFET (407 or 721) or the N-channel MOSFET (408 or 702)) naturally including a source region and a drain region of a first conductivity type formed overlying the insulative layer, a body region disposed between the source region and the drain region and overlying the insulative layer, a gate insulative layer overlying the body region and a gate region overlying the gate insulative layer; a diode (403 or 404; or, 702 or 703) circuit conductively coupled to the source region; and a conductive connection coupling the gate region to the diode circuit. It is noted that the body region in such an SOI MOSFET therein normally naturally comprises a material having a second conductivity type (as evidenced in the prior art such as US 5,892,260; see the P-channel MOSFET or the N-channel MOSFET in Fig. 4).

Regarding claim 11, it is noted that in an SOI structure such as the on in Staab, the insulative layer is normally naturally formed of a buried silicon oxide layer (as further evidenced in the prior art such as US 5,892,260; see the silicon oxide insulative layer 302 in Fig. 4).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Staab in view of Kluth (US 6,521,515).

The disclosure of Staab is discussed as applied to claims 1, 4 and 9-11 above.

The SOI device of Staab further includes a conductive trace connecting the gate region to the diode circuit. And, it is art-known that such a conductive trace is normally commonly formed of a metal material for reducing the interconnection resistance. Although Staab does not expressly disclose that the SOI device can further comprise a conductive region formed overlying the gate electrode, one of ordinary skill in the art would readily recognize that a conductive region can be desirably formed overlying the gate region for reducing the overall resistance of the gate electrode, as evidenced in Kluth (see the metallization layer 24 overlying the gate region 12 in Figs. 1B, 3G and 3F).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the metallization layer of Kluth into the SOI device of Staab, so that an SOI device with reduced gate resistance would be obtained.

9. Claims 5-7 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Staab in view of Williams (EP 0928054A2).

The disclosure of Staab is discussed as applied to claims 1, 4 and 9-11 above.

Although Staab does not expressly disclose that the diode circuit for discharging can comprise a pair of back-to-back diodes, one of ordinary skill in the art would readily recognize that such a discharging diode can be desirable formed of a pair of back-to-back diodes for achieving the desired triggering level of the protective circuit, as evidenced in Williams (see the back-to-back diodes in Figs. 8A and 8B; also see the abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the back-to-back diodes of Williams into the SOI device of Staab, so that an SOI device with desired triggering level in the protective circuit would be obtained.

Regarding claims 7 and 19, it is noted that it is art-known that the individual SOI diodes can be readily formed in silicon islands separated from each other by an insulative region for better performance control of the individual diodes, as further evidenced in Staab (see the insulative region 876 or 877 in Fig. 8b).

Regarding claim 18, the SOI device of Staab further includes a conductive trace connecting the gate region to the diode circuit. And, it is art-known that such a conductive trace is normally commonly formed of a metal material for reducing the interconnection resistance. In addition, it is noted that the top portion of the gate electrode in Staab can be regarded as a conductive region.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Staab in view of Ker et al. ("Ker"; US 2002/0109153).

The disclosure of Staab is discussed as applied to claims 1, 4 and 9-11 above.

Although Staab does not expressly disclose that the diode circuit for discharging can comprise at least three diodes connected in series, one of ordinary skill in the art would readily recognize that such a discharging diode can be desirable formed of least three diodes connected in series for achieving the desired triggering level of the protective circuit, as evidenced in Ker (see the three diodes D1-D3 or D4-D6 in Fig. 12 or 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the series diodes of Ker into the SOI device of Staab, so that an SOI device with desired triggering level in the protective circuit would be obtained.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference D is cited as being related to a SOI MOSFET structure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is (703)306-5729. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SH
September 10, 2003

SHOUXIANG HU
PRIMARY EXAMINER